

<<Correct Hardware Des>>

图书基本信息

书名：<<Correct Hardware Design and Verification Methods正确的硬件设计与验证法/会议录>>

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内容概要

This book constitutes the refereed proceedings of the 13th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, CHARME 2005, held in Saarbrücken, Germany, in October 2005. The 21 revised full papers and 18 short papers presented together with 2 invited talks and one tutorial were carefully reviewed and selected from 79 submissions. The papers are organized in topical sections on functional approaches to design description, game solving approaches, abstraction, algorithms and techniques for speeding (DD-based) verification, real time and LTL model checking, evaluation of SAT-based tools, model reduction, and verification of memory hierarchy mechanisms.

书籍目录

Invited Talks Is Formal Verification Bound to Remain a Junior Partner of Simulation? Verification Challenges in Configurable Processor Design with ASIP MeisterTutorial Towards the Pervasive Verification of Automotive SystemsFunctional Approaches to Design Description Wired: Wire-Aware Circuit Design Formalization of the DE2 LanguageGame Solving Approaches Finding and Fixing Faults Verifying Quantitative Properties Using Bound FunctionsAbstraction How Thorough Is Thorough Enough? Interleaved Invariant Checking with Dynamic Abstraction Automatic Formal Verification of Liveness for Pipelined Processors with Multicycle Functional UnitsAlgorithms and Techniques for Speeding (DD-Based) Verification 1 Efficient Symbolic Simulation via Dynamic Scheduling, Don't Caring, and Case Splitting Achieving Speedups in Distributed Symbolic Reachability Analysis Through Asynchronous Computation Saturation-Based Symbolic Reachability Analysis Using Conjunctive and Disjunctive PartitioningReal Time and LTL Model Checking Real-Time Model Checking Is Really Simple Temporal Modalities for Concisely Capturing Timing Diagrams Regular VacuityAlgorithms and Techniques for Speeding Verification 2 Automatic Generation of Hints for Symbolic Traversal Maximal Input Reduction of Sequential Netlists via Synergistic Reparameterization and Localization Strategies A New SAT-Based Algorithm for Symbolic Trajectory EvaluationEvaluation of SAT-Based ToolsModel ReductionVerification of Memory Hierarchy MechanismsShort PapersAuthor Index

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