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13   ISBN   9783540297901

10   ISBN   3540297901

2006-01-13

Springer

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This book contributes the thoroughly refereed post-proceedings of the 4th International Workshop on Power-Aware Computer Systems, PACS 2004, held in Portland, OR, USA in December 2004. The 12 revised full papers presented were carefully reviewed, selected, and revised for inclusion in the book. The papers span a wide spectrum of topics in power-aware systems; they are organized in topical sections on microarchitecture- and circuit-level techniques, power-aware memory and interconnect systems, and frequency- and voltage-scaling techniques.

Microarchitecture- and　Circuit-Level Techniques　An Optimized Front-End Physical Register File with Banking and　Writeback Filtering　Reducing Delay and Power Consumption of the Wakeup Logic Through　Bit-Sliced Datapath for Energy-Efficient High Performance　Low-Overhead Core Swapping for Thermal ManagementPower-Aware Memory and Interconnect Systems　Energy-Aware Data Prefetching for General-Purpose Programs　Bus Power Estimation and Power-Efficient Bus Arbitration for　Context-Independent Codes for Off-Chip InterconnectsFrequency-Volt age- Scaling Techniques　Effective Dynamic Voltage Scaling Through CPU-Boundedness　Safe Overprovisioning: Using Power Limits to Increase Aggregate Throughput　Power Consumption Breakdown on a Modern LaptopAuthor Index

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