<<2001-高性能计算 - HiPC 2001>>

图书基本信息

书名: <<2001-高性能计算 - HiPC 2001High Performance Computing - HiPC>>

13位ISBN编号: 9783540430094

10位ISBN编号: 3540430091

出版时间:2002-1

出版时间:1edition(2002年1月1日)

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页数:438

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内容概要

This book constitutes the refereed proceedings of the 8th International Conference on High Performance Computing, HiPC 2001, held in Hyderabad, India, in December 2001. The 29 revised full papers presented together with 5 keynote papers and 3 invited papers were carefully reviewed and selected from 108 submissions. The papers are organized in topical sections on algorithms, applications, architecture, systems software, communications networks, and challenges in networking.

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书籍目录

Keynote Address Stability Issues in Heterogeneous and FIFO Networks under the Adversarial Queueing Model Stability Issues in Heterogeneous and FIFO Networks under the Adversarial Queueing Model Session Algorithms Mesh Algorithms for Multiplication and Division Compact Routing in Directed Networks with Stretch Factor of Two Parametric Scheduling - Algorithms and Complexity An Efficient Algorithm for Computing Lower Bounds on Time and Processors for Scheduling Precedence Graphs on MulticomputerSystems On Job Scheduling for HPC-Clusters and the dynP Scheduler An Adaptive Scheme for Fault-Tolerant Scheduling of Soft Real-Time Tasks in Multiproeessor SystemsKeynote Address Learning from the Success of MPI Learning from the Success of MPISession : Applications Gyrokinetic Simulations of Plasma Turbulence on Massively Parallel Computers A Parallel Krylov-Type Method for Nonsymmetric LinearSystems Evolving Cellular Automata Based Associative Memory for Pattern Recognition Efficient Parallel Algorithms and Software for Compressed Octreeswith Applications to Hierarchical Methods A Case Study of Improving Memory Locality in Polygonal Model Simplification: Metrics and PerformanceKeynote Address High-Performance Scalable Java Virtual Machines High-Performance Scalable Java Virtual MachinesSession : Architecture Shared Virtual Memory Clusters with Next-Generation Interconnection Networks and Wide Compute Nodes Stream-Packing: Resource Allocation in Web Server Farmswith a QoS Guarantee Weld: A Multithreading Technique towards Latency-Tolerant VLIW Processors Putting Data Value Predictors to Work in Fine-Grain ParallelProcessors Confidence Estimation for Branch Prediction Reversal Retargetable Program Profiling Using High Level Processor ModelsSession : Systems SoftwareSession :Communication NetworksInvited Session :Advances and Research Challenges in NetworkingAuthor Index

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