

<<时钟发生器在片上系统处理器中的应用>>

图书基本信息

书名：<<时钟发生器在片上系统处理器中的应用>>

13位ISBN编号：9787030188526

10位ISBN编号：7030188527

出版时间：2007-8

出版时间：科学

作者：发伊姆

页数：245

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内容概要

《时钟发生器在片上系统处理器中的应用》针对在SOC芯片上使用的全集成频率合成器的设计，从电路和系统的角度对锁相环的原理和设计进行了分析。

特别是在电路层次上，讨论了深亚微米CMOS数字工艺中的低电压模拟电路的设计，有比较大的参考意义。

在对锁相环基本工作原理分析的基础之上，《时钟发生器在片上系统处理器中的应用》分析了具体的时钟产生方案和电路设计问题，并进一步讨论了锁相环的应用。

《时钟发生器在片上系统处理器中的应用》还包括了PLL可测试性设计的内容。

最后还从宏观角度讨论了SOC时钟域的设计。

书中包含的大量实际问题分析应该有助于读者更好地理解时钟产生器设计中的核心问题。

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编辑推荐

Clock Generators for SOC Processors This book examines the issue of design of fully-integrated frequency synthesizers suitable for system-on-a-chip (soc) processors . This book takes a more global design perspective in jointly examining the design space at the circuit level as well as at the architectural level . The coverage of the book is comprehensive and includes summary chapters on circuit theory as well as feedback control theory relevant to the operation of phase locked loops (PLLs) . On the circuit level , the discussion includes low-voltage analog design in deep submicron digital CMOS processes , effects of supply noise , substrate noise , as well device noise . On the architectural level , the discussion includes PLL analysis using continuous-time as well as discrete-time models , linear and nonlinear effects of PLL performance , and detailed analysis of locking behavior .

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