

## <<计算机体系结构>>

### 图书基本信息

书名：<<计算机体系结构>>

13位ISBN编号：97871111109211

10位ISBN编号：711110921X

出版时间：2003-12-1

出版时间：机械工业出版社

作者：John L.Hennessy,David A.Patterson

页数：883

版权说明：本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问：<http://www.tushu007.com>

## <<计算机体系结构>>

### 内容概要

The third edition of *Computer Architecture: A Quantitative Approach* should have been easy to write. After all, our quantitative approach hasn't changed, and we sought to continue our focus on the basic principles of computer design through two editions. The examples had to be updated, of course, just as we did for the second edition. The dramatic and ongoing advances in the field as well as the creation of new markets for computers and new approaches for those markets, however, led us to rewrite almost the entire book. The pace of innovation in computer architecture continued unabated in the six years since the second edition. As when we wrote the second edition, we found that numerous new concepts needed to be introduced, and other material designated as more basic. Although this is officially the third edition of *Computer Architecture: A Quantitative Approach*, it is really our fifth book in a series that began with the first edition, continued with *Computer Organization and Design: The Hardware/Software Interface (COD:HSI)*, and then the second edition of both books. Over time ideas that were once found here have moved to *COD:HSI* or to background tutorials in the appendices. This migration, combined with our goal to present concepts in the context of the most recent computers, meant there was remarkably little from the second edition that could be preserved intact, and practically nothing is left from the first edition.

## &lt;&lt;计算机体系结构&gt;&gt;

## 书籍目录

Chapter 1 Fundamentals of Computer Design  
 1.1 Introduction  
 1.2 The Changing Face of Computing and the Task of the Computer Designer  
 1.3 Technology Trends  
 1.4 Cost, Price, and Their Trends  
 1.5 Measuring and Reporting Performance  
 1.6 Quantitative Principles of Computer Design  
 1.7 Putting It All Together: Performance and Price-Performance  
 1.8 Another View: Power Consumption and Efficiency as the Metric  
 1.9 Fallacies and Pitfalls  
 1.10 Concluding Remarks  
 1.11 Historical Perspective and References Exercises  
 Chapter 2 Instruction Set Principles and Examples  
 2.1 Introduction  
 2.2 Classifying Instruction Set Architectures  
 2.3 Memory Addressing  
 2.4 Addressing Modes for Signal Processing  
 2.5 Type and Size of Operands  
 2.6 Operands for Media and Signal Processing  
 2.7 Operations in the Instruction Set  
 2.8 Operations for Media and Signal Processing  
 2.9 Instructions for Control Flow  
 2.10 Encoding an Instruction Set  
 2.11 Crosscutting Issues: The Role of Compilers  
 2.12 Putting It All Together: The MIPS Architecture  
 2.13 Another View: The Trimedia TM32 CPU  
 2.14 Fallacies and Pitfalls  
 2.15 Concluding Remarks  
 2.16 Historical Perspective and References Exercises  
 Chapter 3 Instruction-Level Parallelism and Its Dynamic Exploitation  
 3.1 Instruction-Level Parallelism: Concepts and Challenges  
 3.2 Overcoming Data Hazards with Dynamic Scheduling  
 3.3 Dynamic Scheduling: Examples and the Algorithm  
 3.4 Reducing Branch Costs with Dynamic Hardware Prediction  
 3.5 High-Performance Instruction Delivery  
 3.6 Taking Advantage of More ILP with Multiple Issue  
 3.7 Hardware-Based Speculation  
 3.8 Studies of the Limitations of ILP  
 3.9 Limitations on ILP for Realizable Processors  
 3.10 Putting It All Together: The P6 Microarchitecture  
 3.11 Another View: Thread-Level Parallelism  
 3.12 Crosscutting Issues: Using an ILP Data Path to Exploit TLP  
 3.13 Fallacies and Pitfalls  
 3.14 Concluding Remarks  
 3.15 Historical Perspective and References Exercises  
 Chapter 4 Exploiting Instruction-Level Parallelism with Software Approaches  
 4.1 Basic Compiler Techniques for Exposing ILP  
 4.2 Static Branch Prediction  
 4.3 Static Multiple Issue: The VLIW Approach  
 4.4 Advanced Compiler Support for Exposing and Exploiting ILP  
 4.5 Hardware Support for Exposing More Parallelism at Compile Time  
 4.6 Crosscutting Issues: Hardware versus Software Speculation Mechanisms  
 4.7 Putting It All Together: The Intel IA-64 Architecture and Itanium Processor  
 4.8 Another View: ILP in the Embedded and Mobile Markets  
 4.9 Fallacies and Pitfalls  
 4.10 Concluding Remarks  
 4.11 Historical Perspective and References Exercises  
 Chapter 5 Memory Hierarchy Design  
 5.1 Introduction  
 5.2 Review of the ABCs of Caches  
 5.3 Cache Performance  
 5.4 Reducing Cache Miss Penalty  
 5.5 Reducing Miss Rate  
 5.6 Reducing Cache Miss Penalty or Miss Rate via Parallelism  
 5.7 Reducing Hit Time  
 5.8 Main Memory and Organizations for Improving Performance  
 5.9 Memory Technology  
 5.10 Virtual Memory  
 5.11 Protection and Examples of Virtual Memory  
 5.12 Crosscutting Issues: The Design of Memory Hierarchies  
 5.13 Putting It All Together: Alpha 21264 Memory Hierarchy  
 5.14 Another View: The Emotion Engine of the Sony Playstation 2  
 5.15 Another View: The Sun Fire 6800 Server  
 5.16 Fallacies and Pitfalls  
 5.17 Concluding Remarks  
 5.18 Historical Perspective and References Exercises  
 Chapter 6 Multiprocessors and Thread-Level Parallelism  
 6.1 Introduction  
 6.2 Characteristics of Application Domains  
 6.3 Symmetric Shared-Memory Architectures  
 6.4 Performance of Symmetric Shared-Memory Multiprocessors  
 6.5 Distributed Shared-Memory Architectures  
 6.6 Performance of Distributed Shared-Memory Multiprocessors  
 6.7 Synchronization  
 6.8 Models of Memory Consistency: An Introduction  
 6.9 Multithreading: Exploiting Thread-Level Parallelism within a Processor  
 6.10 Crosscutting Issues  
 6.11 Putting It All Together: Sun's Wildfire Prototype  
 6.12 Another View: Multithreading in a Commercial Server  
 6.13 Another View of Embedded Multiprocessors  
 6.14 Fallacies and Pitfalls  
 6.15 Concluding Remarks  
 6.16 Historical Perspective and References Exercises  
 Chapter 7 Storage Systems  
 7.1 Introduction  
 7.2 Types of Storage Devices  
 7.3 Buses--Connecting I/O Devices to CPU/Memory  
 7.4 Reliability, Availability, and Dependability  
 7.5 RAID: Redundant Arrays of Inexpensive Disks  
 7.6 Errors and Failures in Real Systems  
 7.7 I/O Performance Measures  
 7.8 A Little Queuing Theory  
 7.9 Benchmarks of Storage Performance and Availability  
 7.10 Crosscutting Issues  
 7.11 Designing an I/O System in Five Easy Pieces  
 7.12 Putting It All Together: EMC Symmetrix and Celerra  
 7.13 Another View: Sanyo VPC-SX500 Digital Camera  
 7.14 Fallacies and Pitfalls  
 7.15 Concluding Remarks  
 7.16 Historical Perspective and References Exercises  
 Chapter 8 Interconnection Networks and Clusters  
 8.1 Introduction  
 8.2 A Simple Network  
 8.3 Interconnection Network Media  
 8.4 Connecting More Than Two

<<计算机体系结构>>

Computers  
8.5 Network Topology  
8.6 Practical Issues for Commercial Interconnection Networks  
8.7 Examples of Interconnection Networks  
8.8 Internetworking  
8.9 Crosscutting Issues for Interconnection Networks  
8.10 Clusters  
8.11 Designing a Cluster  
8.12 Putting It All Together: The Google Cluster of PCs  
8.13 Another View: Inside a Cell Phone  
8.14 Fallacies and Pitfalls  
8.15 Concluding Remarks  
8.16 Historical Perspective and References  
Exercises  
Appendix A Pipelining: Basic and Intermediate Concepts  
A.1 Introduction  
A.2 The Major Hurdle of Pipelining--Pipeline Hazards  
A.3 How Is Pipelining Implemented?  
A.4 What Makes Pipelining Hard to Implement?  
A.5 Extending the MIPS Pipeline to Handle Multicycle Operations  
A.6 Putting It All Together: The MIPS R4000 Pipeline  
A.7 Another View: The MIPS R4300 Pipeline  
A.8 Crosscutting Issues  
A.9 Fallacies and Pitfalls  
A.10 Concluding Remarks  
A.11 Historical Perspective and References  
Exercises  
Appendix B Solutions to Selected Exercises  
Introduction  
B.1 Chapter 1 Solutions  
B.2 Chapter 2 Solutions  
B.3 Chapter 3 Solutions  
B.4 Chapter 4 Solutions  
B.5 Chapter 5 Solutions  
B.6 Chapter 6 Solutions  
B.7 Chapter 7 Solutions  
B.8 Chapter 8 Solutions  
B.9 Appendix A Solutions  
Online Appendices ([www.mkp.com/CA3/](http://www.mkp.com/CA3/))  
Appendix C A Survey of RISC Architectures for Desktop, Server, and Embedded Computers  
Appendix D An Alternative to RISC: The Intel 80X86  
Appendix E Another Alternative to RISC: The VAX Architecture  
Appendix F The IBM 360/370 Architecture for Mainframe Computer  
Appendix G Vector Processors Revised by Krste Asanovic  
Appendix H Computer Arithmetic by David Goldberg  
Appendix I Implementing Coherence Protocols  
References  
Index

<<计算机体系结构>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:<http://www.tushu007.com>