图书基本信息

- 书名:<<计算机体系结构>>
- 13位ISBN编号:9787111109211
- 10位ISBN编号:711110921X
- 出版时间:2003-12-1
- 出版时间:机械工业出版社
- 作者: John L.Hennessy, David A.Patterson
- 页数:883
- 版权说明:本站所提供下载的PDF图书仅提供预览和简介,请支持正版图书。

第一图书网, tushu007.com

更多资源请访问:http://www.tushu007.com

内容概要

The third edition of Computer Architecture: A Quantitative Approach should have been easy to write. After all, our quantitative approach hasn't changed, and we sought to continue our focus on the basic principles of computer design through two editions. The examples had to be updated, of course, just as we did for the second edition. The dramatic and ongoing advances in the field as well as the creation of new markets for computers and new approaches for those markets, however, led us to rewrite almost the entire book. The pace of innovation in computer architecture continued unabated in the six years since the second edition. As when we wrote the second edition, we found that numerous new concepts needed to be introduced, and other material designated as more basic. Although this is officially the third edition of Computer Architecture: A Quantitative Approach, it is really our fifth book in a series that began with the first edition, continued with Computer Organization and Design: The Hardware/Software Interface (COD:HSI), and then the second edition of both books. Over time ideas that were once found here have moved to COD:HSI or to background tutorials in the appendices. This migration, combined with our goal to present concepts in the context of the most recent computers, meant there was remarkably little from the second edition that could be preserved intact, and practically nothing is left from the first edition.

书籍目录

Chapter 1 Fundamentals of Computer Design1.1 Introduction1.2 The Changing Face of Computing and the Task of the Computer Designer 1.3 Technology Trends 1.4 Cost, Price, and Their Trends 1.5 Measuring and Reporting Performance1.6 Quantitative Principles of Computer Design1.7 Putting It All Together: Performance and Price-Performance1.8 Another View: Power Consumption and Efficiency as the Matric1.9 Fallacies and Pitfalls1.10 Concluding Remarks1.11 Historical Perspective and References ExercisesChapter 2 InStruction Set Prindples and Examples2.1 Introduction2.2 Classifying Instruction Set Architectures2.3 Memory Addressing2.4 Addressing Modes for Signal Processing 2.5 Type and Size of Operands 2.6 Operands for Media and Signal Processing 2.7 Operations in the Instruction Set2.8 Operations for Media and Signal Processing2.9 Instructions for Control Flow2.10 Encoding an Instruction Set2.11 Crosscutting Issues: The Role of Compilers2.12 Putting It All Together: The MIPS Architecture 2.1 3 Another View: The Trimedia TM32 CPU2.14 Fallacies and Pitfalls 2.15 Concluding Remarks2.16 Historical Perspective and ReferencesExercisesChapter 3 Instruction-Level Parallelism and Its Dynamic Exploitation 3.1 Instruction-Level Parallelism: Concepts and Challenges 3.2 Overcoming Data Hazards with Dynamic Scheduling3.3 Dynamic Scheduling: Examples and the Algorithm3.4 Reducing Branch Costs with Dynamic Hardware Prediction 3.5 High-Performance Instruction Delivery 3.6 Taking Advantage of More ILP with Multiple Issue3.7 Hardware-Based Speculation3.8 Studies of the Limitations of ILP3.9 Limitations on ILP for Realizable Processors3.10 Putting It All Together: The P6 Microarchitecture3.11 Another View: Thread-Level Parallelism 3.12 Crosscutting Issues: Using an ILP Data Path to Exploit TLP3.13 Fallacies and Pitfalls3.14 Concluding Remarks3.15 Historical Perspective and ReferencesExercisesChapter 4 Exploiting Instruction-Level Parallelism with Software Approaches4.1 Basic Compiler Techniques for Exposing ILP4.2 Static Branch Prediction 4.3 Static Multiple Issue: The VLIW Approach 4.4 Advanced Compiler Support for Exposing and Exploiting ILP4.5 Hardware Support for Exposing More Parallelism at Compile Time4.6 Crosscutting Issues: Hardware versus SoftwareSpeculation Mechanisms4.7 Putting It All Together: The Intel IA-64 Architecture and Itanium Processor4.8 AnotherView: ILP in the Embedded and Mobile Markets4.9 Fallacies and Pitfalls4.10 Concluding Remarks4.11 Historical Perspective and ReferencesExercisesChapter 5 Memory Hierarchy Design5.1 Introduction 5.2 Review of the ABCs of Caches 5.3 Cache Performance 5.4 Reducing Cache Miss Penalty 5.5 Reducing Miss Rate5.6 Reducing Cache Miss Penalty or Miss Rate via Parallelism5.7 Reducing Hit Time5.8 Main Memory and Organizations for Improving Performance5.9 Memory Technology5.10 Virtual Memory5.11 Protection and Examples of Virtual Memory 5.12 Crosscutting Issues: The Design of Memory Hierarchies 5.13 Putting It All Together: Alpha 21264 Memory Hierarchy5.14 Another View: The Emotion Engine of the Sony Playstation 25.15 Another View: The Sun Fire 6800 Server5.16 Fallacies and Pitfalls5.17 Concluding Remarks5.18 Historical Perspective and ReferencesExercisesChapter 6 Multiprocessors and Thread-Level Parallelism6.1 Introduction 6.2 Characteristics of Application Domains 6.3 Symmetric Shared-Memory Architectures 6.4 Performance of Symmetric Shared-Memory Multiprocessors6.5 Distributed Shared-Memory Architectures6.6 Performance of Distributed Shared-Memory Multiprocessors6.7 Synchronization6.8 Models of Memory Consistency: An Introduction 6.9 Multithreading: Exploiting Thread-Level Parallelism within a Processor 6.10 Crosscutting Issues6.11 Putting It All Together: Sun's Wildfire Prototype6.12 Another View Multithreading in a Commercial Server6.13 Another View f Embedded Multiprocessors6.14 Fallacies and Pitfalls6.15 Concluding Remarks6.16 Historical Perspective and ReferencesExercisesChapter 7 Storage Systems7.1 Introduction7.2 Types of Storage Devices7.3 Buses--Connecting I/O Devices to CPU/Memory7.4 Reliability, Avai1ability, and Dependability7.5 RAID: Redundant Arrays of Inexpensive Disks7.6 Errors and Failures in Real Systems7.7 I/O Performance Measures 7.8 A Little Queuing Theory 7.9 Benchmarks of Storage Performance and Availability 7.10 Crosscutting Issues7.11 Designing an I/O System in Five Easy Pieces7.12 Putting It All Together: EMC Symmetrix and Celerra7.13 Another View: Sanyo VPC-SX500 Digital Camera7.14 Fallacies and Pitfalls7.15 Concluding Remarks7.16 Historical Perspective and ReferencesExercisesChapter 8 Interconnection Networks and Clusters8.1 Introduction8.2 A Simple Network8.3 Interconnection Network Media8.4 Connecting More Than Two

Computers8.5 Network Topology8.6 Practical Issues for Commercial Interconnection Networks8.7 Examples of Interconnection Networks8.8 Internetworking8.9 Crosscutting Issues for Interconnection Networks8.10 Clusters8.11 Designing a C1uster8.12 Putting It All Together: The Google Cluster of PCs8.13 Another View: Inside a Cell Phone8.14 Fallacies and Pitfalls8.15 Concluding Remarks8.16 Historical Perspective and ReferencesExercisesAppendix A Pipelining: Basic and Intermediate ConceptsA.1 IntroductionA.2 The Major Hurdle of Pipelining--Pipeline HazardsA.3 How Is Pipelining Implemented?A.4 What Makes Pipelining Hard to Implement?A.5 Extending the MIPS Pipeline to Handle Multicycle OperationsA.6 Putting It All Together: The MIPS R4000 PipelineA.7 Another View: The MIPS R4300 PipelineA.8 Crosscutting IssuesA.9 Fallacies and PitfallsA.10 Concluding RemarksA.11 Historical Perspective and ReferencesExercisesAppendix B Solutions to Selected ExercisesIntroductionB.1 Chapter 1 SolutionsB.2 Chapter 2 SolutionsB.3 Chapter 3 SolutionsB.4 Chapter 4 SolutionsB.5 Chapter 5 SolutionsB.6 Chapter 6 SolutionsB.7 Chapter 7 SolutionsB.8 Chapter 8 SolutionsB.9 Appendix A SolutionsOnline Appendices (www.mkp.com/CA3/)Appendix C A Survey of RISC Architectures for Desktop, Server, and Embedded ComputersAppendix D An Alternative to RISC: The Intel 80X86Appendix E Another Alternative to RISC: The VAX Architecture Appendix F The IBM 360/370 Architecture for Mainframe ComputerAppendix G Vector ProcessorsRevised by Krste AsanovicAppendix H Computer Arithmoticby David GoldbergAppendix I Implementing Coherence ProtocolsReferencesIndex



版权说明

本站所提供下载的PDF图书仅提供预览和简介,请支持正版图书。

更多资源请访问:http://www.tushu007.com