<<高速CMOS电路设计>>

图书基本信息

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前言

The method of logical effort is a way of thinking about delay in Mos circuits. It seeks to determine quickly a circuits maximum possible speed and how to achieve it. It provides insight into how both the sizes of different transistors and the circuit topology itself affect circuit delay. We offer two new names for causes of delay in Mos circuits, electrical effort and logical effort. The similarity of these names reflects a remarkable symmetry between the effort required to drive an electrical load and the effort required to perform a logic function; the two forms of effort present identical and inter- changeable sources of delay. Identifying these concepts leads to a formulation that simplifies circuit analysis and allows a designer to analyze alternative circuit designs quickly. Electrical effort is a new name for the problem overcome by electrical gain. It has long been known that the fastest driver for a large electrical load is a multistage amplifier whose gain is distributed among stages of exponentially increasing size. Thinking of what amplifiers do as compensating for electrical effort paves the way to understanding how they similarly compensate for logical effort.

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内容概要

《高速CMOS电路设计Logical Effirt方法(英文版)》讲述如何获得高速CMOS电路，这正是高速集成电路设计师们渴望获得的技术。
在设计中，我们往往面对无数的选择，《高速CMOS电路设计Logical Effirt方法(英文版)》将告诉我们如何将这些选择变得更容易和更有技巧。
《高速CMOS电路设计Logical Effirt方法(英文版)》提供了一个简单而普遍有效的方法，用于估计拓扑、电容等因素造成的延迟。
《高速CMOS电路设计Logical Effirt方法(英文版)》实用性强，适合集成电路设计师以及相关专业的师生。

作者简介

Ivan Sutherland，著名计算机科学家。
因对计算机图形学和电子设计领域的开创性贡献先后获得1988年图灵奖和1998年冯·诺依曼奖。
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曾参与Intel安腾和奔腾II的电路设计。
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章节摘录

To set the context of the problems addressed by logical effort, we begin by reviewing a simple integrated circuit design flow. We will see that topology selection and gate sizing are key steps of the flow. Without a systematic approach, these steps are extremely tedious and time-consuming. Logical effort offers such an approach to these problems. Figure I. 1 shows a simplified chip design flow illustrating the logic, circuit, and physical design stages. The design starts with a specification, typically in textual form, defining the functionality and performance targets of the chip. Most chips are partitioned into more manageable blocks so that they may be divided among multiple designers and analyzed in pieces by CAD tools. Logic designers write register transfer level （RTL） descriptions of each block in a language like Verilog or VHDL and simulate these models until they are convinced the specification is correct. Based on the complexity of the RTL descriptions, the designers estimate the size of each block and create a floorplan showing relative placement of the blocks. The floorplan allows wire-length estimates and provides goals for the physical design. Given the RTL and floorplan, circuit design may begin. There are two general styles of circuit design: custom and automatic. Custom design trades additional human labor for better performance. In a custom methodology, the circuit designer has flexibility to create cells at a transistor level or choose from a library of predefined cells. The designer must make many decisions: Should I use static CMOS, transmission gate logic, domino circuits, or other circuit families ?
What circuit topology best implements the functions specified in theRTL ?

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