第一图书网, tushu007.com

<<计算机系统体系结构>>

图书基本信息

书名：<<计算机系统体系结构>>

13位ISBN编号：9787302028314

10位ISBN编号：7302028311

出版时间：2000-10

出版时间：清华大学出版社

作者：M.Morris Mano

页数：523

版权说明：本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问：http://www.tushu007.com

第一图书网, tushu007.com

<<计算机系统体系结构>>

内容概要

本书介绍计算机体系结构以及计算机组织与设计，向读者提供掌握计算机硬件操作所必需的基本知识。
内容包括：用于计算机组织和设计的各种部件；设计一台计算机的详细步骤：中央处理机，输入/输出及存储器的组织与体系结构；多处理概念。
全书分13章：1.数字逻辑电路，2.数字部件。
3.数据表示法，4.寄存器传输与微操作，5.基本计算机组织与设计，6.基本计算机的程序设计，7.微程序控制，8.中央处理机，9.流水处理与向量处理，10.计算机体系结构，11.输入/输出组织，12.存储器组织，13.多处理机。
本书可作电气工程，计算机工程或计算机科学系的“计算机硬件系统”课的教材，还可作工程技术及科研人员了解计算机硬件体系结构基本知识的自学参考书。

第一图书网, tushu007.com

<<计算机系统体系结构>>

书籍目录

CHAPTER ONE Digital Logic Circuits1-1 Digtal Computers1-2 Logic Gates1-3 Boolean AlgebraComplement of a Function1-4 Map SimplificationProduct-of-Sums SimplificationDon ’ t-Care Conditions1-5 Combinational CircuitsHalf-AdderFull-Adder1-6 Flip-FlopsSR Flip-FlopsD Flip-FlopsJK Flip-FlopsT Flip-FlopsEdge-Triggered Flip-FlopsExctiation Tables1-7 Sequential CircuitsFlip-Flops Input EquationsState TableState DiagramDesign ExampleDesign ProcedureProblemsReferencesCHAPTER TWO Digital Components2-1 Integrated Circuits2-2 DecodersNAND Gate DecoderDecoder ExpansionEncoders2-3 Multiplexers2-4 RegistersRegister with Parallel Load2-5 Shift RegistersBidirectional Shift Register with Parallel Load2-6 Binary CountersBinary Counters with Parallel Load2-7 Memory UnitRandom-Access MemoryRead-Only MemoryTypes of ROMsProblemsReferencesCHAPTER THREE Data Representation3-1 Data TypesNumber SystemsOctal and Hexadecimal NumbersDecimal RepresentationAlphanumeric Representation3-2 Complements(r-1) ’ s Complement(r ’ s) ComplementSubtraction of Unsigned Numbers3-3 Fixed-Point RepresentationInteger RepresentationArithmetic AdditionArithmetic SubtractionOverflowDecimal Fixed-Point Representation3-4 Floating-Point Representation3-5 Other Binary CodesGray CodeOther Decimal CodesOther Alphanumeric Codes3-6 Error Detection CodesProblemsReferencesCHAPTER FOUR Register Transfer and Microoperations4-1 Register Transfer Language4-2 Register Transfer4-3 Bus and Memory TransfersThree-State Bus BuffersMemory Transfer4-4 Arithmetic MicrooperationsBinary AdderBinary Adder-SubtractorBinary IncrementerArithmetic Circuit4-5 Logic MicrooperationsList of Logic MicrooperationsHardware ImplementationSome Applications4-6 Shift MicrooperationsHardware Implementation4-7 Arithmetic Logic Shift UnitProblemsReferencesCHAPTER FIVE Basic Computer Organization and Design5-1 Instruction CodesStored Program OrganizationIndirect Address5-2 Computer registersCommon Bus System5-3 Computer ImstructionsInstruction Set Completeness5-4 Timing and Control5-5 Instruction CycleFetch and DecodeDetermine the Type of InstructionRegister-Reference Instructions5-6 Memory-Reference InstructionsAND to ACADD to ACLDA:Load to ACSTA: Store ACBUN:Branch UnconditionallyBSA:Rranch and Save return AddressISZ:Increment and Skip If ZeroControl Flowchart5-7 Input-Output and InterruptInput-Output ConfigurationInput-Output InstructionsProgram InterruptImterrupt Cycle5-8 Complete Computer Description5-9 Design of Basic ComputerControl Logic GatesControl of Registers and MemoryControl of Single Flip-FlopsControl of Common Bus5-10 Design of Accumulator LogicControl of AC RegisterAdder and Logic CircuitProblemsReferencesCHAPTER SIX Programming the Basic Computer6-1 Introduction6-2 Machine Language6-3 Assembly LanguageRules of the LanguageAn ExampleTranslation to Binary6-4 The AssemblerRepresentation of Symbolic Program in MemoryFirst PassSecond Pass6-5 Program Loops6-6 Programming Arithmetic and Logic OperationsMultiplication ProgramDouble-Precision AdditionLogic OperationsShift Operations6-7 SubroutinesSubroutines Parameters and Data Linkage6-8 Input-Output ProgrammingCharacter ManipulationProgram InterruptProblemsReferencesCHAPTER SEVEN Microprogrammed Control7-1 Control Memory7-2 Address SequencingConditional BranchingMapping of InstructionSubroutines7-3 Microprogram ExampleComputer ConfigurationMicroinstruction FormatSymbolic MicroinstructionSThe Fetch RoutineSymbolic MicroprogramBinary Microprogram7-4 Design of Control UnitMicroprogram SequencerProbolemsReferencesCHAPTER EIGHT Central Processing Unit8-1 Introduction8-2 General Register OrganizationControl WordExamples of Microoperations8-3 Stack OrganizationRegister StackMemory StackReverse Polish NotationEvaluation of Arithmetic Expressions8-4 Instruction FormatsThree-Address InstructionsTwo-Address InstructionsOne-Address InstructionsZero-Address InstructionsRISC Instructions8-5 Addressing ModesNumerical Example8-6 Data Transfer and ManipulationData Transfer InstructionsData Manipulation InstructionsArithmetic InstructionsLogical and Bit Manipulation InstructionsShift Instructions8-7 Program ControlStatus Bit ConditionsConditional Branch InstructionsSubroutine Call and RetumProgram InterruptTypes of Interrupts8-8 Reduced Instruction Set Computer(RISC)CISC CharacteristicsRISC CharacteristicsOverlapped Register WindowsBerkeley RISC

第一图书网, tushu007.com

IProblemsReferencesCHAPTER NINE Pipeline and Vector Processing9-1 Parallel Processing9-2 PipeliningGeneral Considerations9-3 Arithmetic Pipeline9-4 Instruction PipelineExample:Four-Segment Instruction PiplineData DependencyHanding of Branch Instructions9-5 RISC PipelineExample:Three-Segment Instruction PipelineDelayed LoadDelayed Branch9-6 Vector ProcessingVector OperationsMatrix MultiplcationMemory InterleavingSupercomputers9-7 Array ProcessorsAttached Array ProcessorSIMD Array ProcessorProblemsReferencesCHAPTER TEN Computer Arithmetic10-1 Introduction10-2 Addition and SubtractionAddition and Subtraction with Signed-Magnitude DataHardware ImplementationHardware AlgorithmAddition and Subtraction with Signed-2 ’ s Complement Data10-3 Multiplication AlgorithmsHardware AlgorithmArray Multiplier10-4 Division AlgorithmsHardware Implementation for Signed-Magnitude DataDivide OverflowHardware AlgorithmOther Algorithms10-5 Floating-Point Arithmetic OperationsBasic ConsiderationsRegister ConsiderationsAddition and SubtractionMultiplicationDivision10-6 Decimal Arithmetic UnitBCD AdderBCD Subtraction10-7 Decimal Arithmetic OperationsAddition and SubtractionMultiplicationDivisionFloating-Point OperationsProblemsReferencesCHAPTER ELEVEN Input-Output Organization11-1 Peripheral DevicesASCII Alphanumeric Characters11-2 Input-Output InterfaceI/O Bus and Interface ModulesI/O versus Memory BusIsolated versus Memory-Mapped I/OExample of I/O Interface11-3 Asynchronous Data TransferStrobe ControlHandshakingAsynchronous Serial TransferAsynchronous Communication InterfaceFirst-In,First-Out Buffer11-4 Modes of TransferExample of Programmed I/OInterrupt-Initiated I/OSoftware Considerations11-5 Priority InterruptDaisy-Chaining PriorityParallel Priority InterruptPriority EncoderInterrupt CycleSoftware RoutinesInitial and Final Operations11-6 Direct Memory Access(DMA)DMA ControllerDMA Transfer11-7 Input-Output PROCessor(IOP)CPU-IOP CommunicationIBM 370 I/O ChannelIntel 8089 IOP11-8 Serial CommunicationCharacter-Oriented ProtocolTransmission ExampleData TransparencyBit-Oriented ProtocolProblemsReferencesCHAPTER TWELVE Memory Organization12-1 Memory Hierarchy12-2 Main MemoryRAM and ROM ChipsMemory Address MapMemory Connecton to CPU12-3 Auxiliary MemoryMagnetic DisksMagnetic Tape12-4 Associative MemoryHardware OrganizationMatch LogicRead OperationWrite Operation12-5 Cache MemoryAssociative MappingDirect MappingSet-Associative MappingWriting into CacheCache Initialization12-6 Virtual MemoryAddress Space and Memory SpaceAddress Mapping Using PagesAssociative Memory Page TablePage Replacement12-7 Memory Management HardwareSegmented-Page MappingNumerical ExampleMemory ProtectionProblemsReferencesCHAPTER THIRTEEN Multiprocessors13-1 Characteristics of Multiprocessors13-2 Interconnection StructuresTime-Shared Common BusMultiport MemoryCrossbar SwitchMultistage Switching NetworkHypercube Interconnection13-3 Interprocessor ArbitrationSystem BusSerial Arbitration ProcedureParallel Arbitration LogicDynamic Arbitration Algorithms13-4 Interprocessor Communication and SynchronizationInterprocessor SynchronizationMutual Exclusion with a Semaphore13-5 Cache CoherenceConditions for IncoherenceSolutions to the Cache Coherence ProblemProblemsReferencesIndex

第一图书网, tushu007.com

<<计算机系统体系结构>>

版权说明

本站所提供下载的PDF图书仅提供预览和简介，请支持正版图书。

更多资源请访问:http://www.tushu007.com