

## <<3维超大规模集成电路>>

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## <<3维超大规模集成电路>>

### 内容概要

本书提出一种新的3维超大规模电路集成方案，即2.5维集成。

根据这一集成方案实现的电子系统将由多层单片集成芯片叠加而成，芯片间将由极细小尺度的“垂直联线”实现电气连接。

这一新集成方案能够在很大程度上克服积累成品率损失的问题。

本书从制造成本和设计系统性能两方面探讨2.5维集成的可行性。

首先，作者建立了一个成本分析模型来比较各种典型集成方案，分析数据表明2.5维集成具备制造成本上的优越性。

从设计性能角度，作者完成了全定制和专用集成电路两种设计风格的一系列设计实例研究，从而证明了2.5维集成能够实现传统单片集成不能达到的系统性能。

同时，为了实现2.5维/3维集成电路版图，作者也开发了第一代2.5维/3维物理设计EDA工具。

本书适合集成电路工艺开发人员和决策人士、集成电路设计人员、电子设计自动化研发人员和决策人士参考。

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