<<专用集成电路时程序验证>>

图书基本信息

书名：<<专用集成电路时程序验证>>

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前言

微电子技术是信息科学技术的核心技术之一，微电子产业是当代高新技术产业群的核心和维护国家主权、保障国家安全的战略性产业。

我国在《信息产业“十五”计划纲要》中明确提出：坚持自主发展，增强创新能力和核心竞争力，掌握以集成电路和软件技术为重点的信息产业的核心技术，提高具有自主知识产权产品的比重。

发展集成电路技术的关键之一是培养具有国际竞争力的专业人才。

微电子技术发展迅速，内容更新快，而我国微电子专业图书数量少，且内容和体系不能反映科技发展的水平，不能满足培养人才的需求，为此，我们系统挑选了一批国外经典教材和前沿著作，组织分批出版。

图书选择的几个基本原则是：在本领域内广泛采用，有很大影响力；内容反映科技的最新发展，所述内容是本领域的研究热点；编写和体系与国内现有图书差别较大，能对我国微电子教育改革有所启示。

本套丛书还侧重于微电子技术的实用性，选取了一批集成电路设计方面的工程技术用书，使读者能方便地应用于实践。

我们真诚地希望，这套丛书能对国内高校师生、工程技术人员以及科研人员的学习和工作有所帮助，对推动我国集成电路的发展有所促进。

也衷心期望着广大读者对我们一如既往的关怀和支持，鼓励我们出版更多、更好的图书。

内容概要

《专用集成电路时序验证》是近10年来惟一一本专门讨论时序及时序验证的专著，共分4章。《专用集成电路时序验证》全面讨论了静态时序验证的各方面内容；全书不仅紧密结合电路图和波形图进行讲解，还结合Synopsys公司的逻辑综合和静态时序分析工具讲解如何通过命令加以实现；介绍过程中不仅从理论上阐述了延迟模型，而且注重实践环节，引入了大量实际示例加以深入探讨。这种写作风格将促进读者能够更全面、细致地理解所讲内容，因此《专用集成电路时序验证》十分适合自学。

作者简介

内库加（Farzad Nekoogar） is Director of Design Services at SiliconDesigns International. Farzad has extensive practical expe-rience verifying timing ofASICs， FPGAs， and systems-on-a-chip. He is the author of Digital Control Using Digital Sig-nal Processing， published by Prentice Hall PTR. He has lec-tured at the University of California at Berkeley on signalprocessing， control systems， and theoretical physics （specifi-cally， Superstring Theory）. He is currently a lecturer at theDepartment of Applied Science at the University of Califor-nia at Davis. Farzad， seen here in December 1992 at Stanford University， with Sir Roger Penrose.Farzad writes： "In this book we try to solve timing issues related to design of micro-chips. I am honored to be pictured here with Sir Roger Penrose， one of the most bril-liant scientists of all time， who has authored some of the most complex theories aboutspace-time， contributing a lot to our understanding of the universe."

书籍目录

章节摘录

Table 1.3 reveals how the input signals determine which paththrough the circuit drives the output. Whenever the input signal e is ne, the values of the other input signals are irrelevant because theone on input e forces the output of the NOR gate to zero. Essentiallythe same situation occurs on line 2 of Table 1.3. The value on input ddetermines the output value. Line 3 shows the conditions where theoutput depends on input a. Line 4 is a more interesting case becausethe path to the output depends on the order of input signal transi-tions. If the input signals are 00000 then become 10000, the transi-tion goes through path cl-c2-c4-c5-c6. The transition 11000 to 10000takes the c2-c4-c5-c6 path while the 10100 to 10000 transition goesthrough the c3-c4-c5-c6 path. In this circuit, the delays from b-outand c-out are the same, but gate and interconnect delays could bedifferent and change the result. The inputs of lines 5 and 6 activatelogic that forces the paths c-out and b-out respectively to determinethe output value. The slowest path between b-out and c-out deter-mines the delay in line 7 only if the transition is from 10000 to11100. The delay path is already set and possibly settled with transi-tions from 10100 to 11100 （c-out） and 11000 to 11100 （b-out）. As a result of understanding the circuits response to inputstimuli, the timing analyzer knows that every path is capable ofproducing a response at the output, so it must consider all pathswhen determining delay. In this specific case, the longest path isfrom a-out through c 1-c2-c4-c5-c6 and it is traversed during two dif-ferent transitions: lines 3 and 4. In chapter 2 we will consider false paths. False paths are logicpaths that are not synthesized because they are functionallyblocked. These paths are recognized by static timing analyzers asunconstrained paths. One example of false paths is the clocks thatare not harmonically related to each other.

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